IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re:	McBride et al.	:	Date: 01 June 2006
Group Art Unit:	2663	:	IBM Corporation
Examiner:	Jonathan Liou	:	Intellectual Property Law
Serial No.:	10/006,604	:	Dept. 917A
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Title: CACHE LINE CUT THROUGH OF LIMITED LIFE DATA IN A DATA PROCESSING SYSTEM

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Karuna Ojanen, Reg. No. 32,484

Dear Sir:

AMENDMENT UNDER 37 CFR 1.111

INTRODUCTORY COMMENTS

In response to the Examiner's Action mailed 21 March 2006 with a shortened statutory period set to expire on 21 June 2006, Applicants submit the following amendments to the claims and remarks.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks are included on pages 8 through 16 of this paper.

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method to forward network data in a data processing system, comprising:

(a) receiving network data into the data processing system, the data processing system comprising a plurality of processing elements, a local SRAM memory, and a cache connected to the local SRAM memory and the plurality of processing elements;

(b) separating the network data into transient portions which are short-lived, and will be modified by one of the plurality of processing elements but whose modifications will not be needed by the data processing system and into portions which will not be modified;

(c) storing both portions of the network packet in ~~a~~ the local SRAM memory;

(d) forwarding the ~~modifiable~~ transient portions of the network data to ~~a~~ the cache connected to and associated with ~~a~~ the plurality of processing elements, one of the plurality of processing ~~element~~ elements requesting ~~at least the modifiable~~ the transient portion of the data;

(e) determining a next ~~processing element~~ destination data processing system of the network data;

(f) transferring the portion of the network data that are not modified to a next SRAM memory ~~subsystem~~ of the next destination data processing ~~element destination~~ system;

(g) modifying the ~~modifiable~~ transient portions within the requesting processing element;

(h) writing back the ~~modified~~ transient portion of the network data to the next SRAM memory of the next destination data processing ~~element destination~~ system independently of transferring the nonmodifiable portion of the network data, and bypassing the local SRAM memory.

2. (Currently Amended) The method of claim 1, wherein the ~~modifiable~~ transient portion of the network data is a packet header of one network protocol which is modified to that of another network protocol.

3. (Previously Amended) The method of claim 2 wherein one network protocol is ATM.

4. (Currently Amended) The method of ~~claims~~ claim 2 wherein one network protocol is ethernet.

5. (Previously Amended) The method of claim 2 wherein one network protocol is PPP, point-to-point protocol.

6. (Currently Amended) The method of ~~claims~~ claim 2 wherein one network protocol is IP, internet protocol.

7. (Currently Amended) The method of claim 2, further comprising:

(a) translating an address if the requesting processing element and the next destination data processing ~~element destination have~~ system have different addresses of the local SRAM memory.

8. (Currently Amended) The method of claim 1, wherein the modification comprises updating an address to that of the next destination data processing system ~~element destination~~.

9. (Original) The method of claim 1, wherein the modification occurs in a network processor.

10. (Original) The method of claim 1, wherein the modification occurs in a local processing element.

11. (Original) The method of claim 1, wherein the modification occurs in an embedded processor in an application specific integrated circuit, ASIC.

12. (Currently Amended) ~~An apparatus~~ A data processing system for data communications, comprising:

(a) a network interface through which to receive incoming data comprised of at least one data packet, the data packet having a modifiable portion and a portion that need not be modified;

(b) a local memory connected to the network interface, the local memory for ~~receiving the data and~~ storing the ~~modifiable portion from the portion that need not be modified~~ incoming data;

(c) a bus interface connected to the local memory which forwards the portion of the data packet that need not be modified to an interconnect fabric, independent of the modifiable portion of the data packet, and to a next local memory of a next processing element system;

(d) a cache in which to store the modifiable portion of the data packet;

(e) a modifier which receives the modifiable portion of the data packet from the cache, updates the modifiable portion of the data packet and forwards the updated modifiable portion of the data packet to the cache and the bus interface that transfers the updated modifiable portion of the data packet to the interconnect fabric, independent of the portion of the data packet that need not be modified, to the next local memory of a next processing element system.

13. (Original) The apparatus of claim 12, wherein the incoming data is digital electrical and/or optical data.

14. (Original) The apparatus of claim 12, wherein the incoming data is analog electrical and/or optical data.

15. (Currently Amended) A memory bypass mechanism, comprising:

(a) means to receive optical and/or digital data;

(b) means to separate the received data into a modifiable portion and a non-modifiable portion;

(c) means to store the received data in a local memory ~~associated with a means to modify the modifiable portion of the received data~~;

(d) means to forward the modifiable portion of the data to a cache associated with a plurality of ~~the~~ modifying means;

(e) means to forward the non-modifiable portion to a next local memory of a destination means to receive the optical and/or digital data:

(f) means to modify the modifiable portion in one of the plurality of modifying means associated with and connected to the cache; and

(g) means to forward the modified portion of data to the cache and then directly to the next memory of the destination means bypassing storing the modified portion in the local memory ~~associated with a means to modify the modifiable portion of the received data~~.

16. (Original) The memory bypass mechanism of claim 15, wherein the modifiable portion of the received data is a header stating a network protocol of the data and/or a destination address of the received data.

17. (Original) The memory bypass mechanism of claim 16, wherein the received header is of a first network protocol and the modified header is a second network protocol.

18. (Original) The memory bypass mechanism of claim 17, wherein the first and second network protocols are selected from the group consisting of: asynchronous transfer mode, ethernet, Internet protocol, and Point-to-Point protocol.

19. (Original) The memory bypass mechanism of claim 15, wherein the modifying means is a processing element in a network processor.

Claims 20 and 21 (Cancelled)

REMARKS

The application was filed on 05 December 2001 with twenty-one claims. The Examiner examined the application and on 09 September 2005 issued a first Action wherein claims 1-10 and 12 were rejected under 35 U.S.C. §102(e) by U.S. Patent Application Publication No. 2003/0067934 A1 entitled MULTIPROTOCOL DECAPSULATION/ENCAPSULATION CONTROL STRUCTURE AND PACKET PROTOCOL CONVERSION METHOD to Hooper et al. (Hooper '934); claim 11 was rejected under 35 U.S.C. §103(a) as being unpatentable over Hooper '934 and U.S. Patent No. 6,754,662 entitled METHOD AND APPARATUS FOR FAST AND CONSISTENT PACKET CLASSIFICATION VIA EFFICIENT HASH-CACHING to Li (Li '662); claims 13-21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hooper '934 and U.S. Patent Application Publication No. 2002/0027901 A1 entitled APPARATUS, METHODS AND SYSTEMS FOR ANONYMOUS COMMUNICATION to Liu (Liu '901). Applicants amended the independent claims and cancelled claims 20 and 21.

The Examiner responded and finally rejected claims 1-10, 12 under 35 U.S.C. §103(a) over Hooper '934 in view of U.S. Patent 6,075,790 entitled ASYNCHRONOUS TRANSFER MODE SYSTEM FOR, AND METHOD OF, WRITING A CELL PAYLOAD BETWEEN A CONTROL QUEUE ON ONE SIDE OF A SYSTEM BUS AND A STATUS QUEUE ON THE OTHER SIDE OF THE SYSTEM BUS to Lincoln et al. (Lincoln '790); claim 11 under 35 U.S.C. §103(a) as being obvious over Hooper '934 in view of Lincoln '790 and further in view of Li '662; claims 13-21 under 35 U.S.C. §103(a) over Lincoln '790 in view of Liu '901. The Examiner objected to claims 5 and 6. Applicants amended claims 3-6 and traversed the substantive art rejections.

The Examiner was persuaded by the traversal and withdrew the finality of the rejection. Now, however, he rejects claims 1-6, 9-10, and 12 under 35 U.S.C. §103(a) as being obvious in view of U.S. Patent No. 6,700,888 entitled MANIPULATING HEADER FIELDS FOR IMPROVED PERFORMANCE IN PACKET COMMUNICATIONS to Jonsson et al. (Jonsson '888); claims 7-8 under 35 U.S.C. §103(a) as being obvious in view of Jonsson '888 in view of Lincoln '790, and claim 11 under 35

U.S.C. §103(a) as being obvious in view of Jonsson '888 in view of Li '662. Claims 13-15 and 17-19 are also rejected under 35 U.S.C. §103(a) as being obvious in view of Jonsson '888 in view of Liu '901, and claim 16 is rejected under 35 U.S.C. §103(a) as being obvious in view of Jonsson '888 in view of Liu '901 and further in view of Lincoln '790. Thus, the Examiner rejects all the claims using the Jonsson '888 patent as a primary reference. The Examiner also objected to claims 4 and 6 because of some informalities. Applicants have amended claims 4 and 6 to remove the objection, and have further amended the independent and pertinent dependent claims although Applicants assert that the amendments are not necessary to overcome the substantive art rejections. Claims 1-19 are pending.

In amending the claims, Applicants have not added new matter. Support in the originally filed specification for the data processing system comprising a plurality of processing elements, a local SRAM memory, and a cache connected to the local SRAM memory and the plurality of processing elements is given in, *inter alia*, Figures 2, 3, and 4 and again on page 9, lines 15-17 and page 11, lines 26-29. Support in the originally filed specification for transient portions that are modified being short-lived and not needed by the data processing system is given at page 13, lines 9-11. Support in the originally filed specification for the next destination data processing system having a SRAM memory is given in Figure 4 and again on page 14, line 26 through page 15, line 2.

The Rejection of claims over Jonsson '888

The Examiner rejected claims 1-6, 9-10 and 12 under 35 U.S.C. §103(a) as being unpatentable over Jonsson '888. Jonsson '888 teaches a data communication method and an apparatus that separates a header from a payload. After separation, the payload is stored in a buffer. The header, having fields that are problematic for compression, may be modified in a field processor. Jonsson' 888 recognized that the integrity of the header may be violated so long as the functionality of the header is maintained by the modifications; specifically two header fields are problematic for compression but these two fields may be changed without affecting the functionality of each: an identification field that identifies the

different parts of packets that have been split into fragments; and a time-to-live/hop-limit field that may be decreased by one for every hop in the path taken by a packet. The gist of Jonsson '888, then is to determine the extent of the modifications of these two fields: if the changes to the header are beyond a threshold, either in sensitivity or in the bit error rate, then changes need be made to the checksum. In any event, changes to the header must be transparent to the header compression node (HCN). After modification, the header is reassembled and then recombined with the payload in the combiner. The reassembled packet stream, i.e., both header/packet, are transmitted to the header compression node (HCN), and from there to the header decompression node. Jonsson '888 states that the header compression node and the header decompression node are embodiments of any type of point-to-point packet communication path.

In order to support the obviousness rejection, the Examiner adds two memories to Jonsson '888, both of which the Examiner says are obvious but neither of which are suggested by any reference. First, the Examiner states that it would be obvious to add a local memory to Jonsson '888 in which to store the packet stream before the header is extracted from the payload. The local memory is analogous to Applicants' claimed local SRAM memory. The Examiner also adds a second local memory to the combiner to store both the payload and the modified header before the recombined packet is transmitted to the header compression node. This memory is analogous to the claimed local memory in the destination processing system. The crux of the rejection relies on equating the combiner with Applicants' claimed next destination processing system in which the modified header goes to the combiner independently of transferring the payload to the combiner and then adding the two memories that don't exist and are not suggested.

Applicants have amended the claims to particularly point out and distinctively claim that network data goes from one processing system having a SRAM, an interconnected cache, and plurality of processing elements to another processing system having a SRAM, an interconnected cache, and a plurality of processing elements. Recall that Applicants recognized that cache coherence, usually a necessity when a processing system has a local memory and a cache, was not necessary and even undesirable when the local processing system would never see the data again and the time required to maintain cache/memory coherence would take away from other processing tasks, such as processing yet another packet.

Jonsson '888 neither teaches nor suggests a cache connected to its field processors; not one word about the importance or disadvantages of maintaining cache coherency between a cache and a local SRAM memory. Jonsson '888, moreover, teaches no local SRAM memory. It is an established principle of patent law that the references themselves must suggest the modification proffered by the Examiner to establish a prima facie case of obviousness. Jonsson '888 makes no such suggestion; therefore, no prima facie assertion of obviousness has been established.

Why doesn't Jonnson '888 teach a cache connected to the field processors? Jonnson '888 is concerned with a very different problem than the one which is solved by Applicants' claimed invention. Jonnson '888 is more concerned with problematic fields of a header during compression - something that Applicants don't even mention. Applicants are more concerned with minimizing memory bandwidth and decreasing memory latencies when transferring data between processing systems - something that Jonsson '888 doesn't even consider.

Applicants take particular exception to the modification posited by the Examiner that the combiner of Jonsson '888 have a local SRAM memory into which both the modified transient portion and the nonmodified portions of the data are reassembled. There is simply no reason for nor any suggestion that the combiner in Jonsson '888 have a local SRAM memory. Jonnson '888 teaches that the payload is already stored in a buffer; from the buffer it is combined with a

modified header for transmission to a header compression node. Why would there be a need for an additional SRAM memory in the combiner when the payload is in a buffer and the purpose of the combiner is to combine header and payload as rapidly as possible?

In another aspect, the payload is not transferred to the combiner independent of the modified header in Jonsson '888, contrary to the claimed apparatus and method of Applicants. Note that the header is reassembled and then, along with the payload, the header is combined with the payload in the combiner. In order to be properly combined for compression, both the header and payload must be transferred to the combiner together. There is no suggestion from Jonsson '888 that the payload waits in the combiner for the modified header and is then combined with the header before compression. Rather, the payload waits in its buffer and when the modified header is reassembled, both the payload and the header are input to the combiner together, not independently.

Thus, Jonsson '888 does not suggest a cache associated with its field processors, as Applicants have claimed. Jonsson '888 does not suggest a local SRAM memory in the combiner, as Applicants have claimed that the destination processing system have a local memory. Lastly, Jonsson '888 does not suggest nor teach that the payload, the unmodified portion of the packet, is transferred to the combiner independently of the header, the modified portion. Indeed, Jonsson '888 teaches exactly the opposite. Respectfully, Applicants have given three claim limitations that are not shown by nor suggested by Jonsson '888. Please remove the rejection of claims 1-6, 9-10 and 12 under 35 U.S.C. §103(a) as being unpatentable over Jonsson '888.

The Rejection of claims 7-8 over Jonsson '888 in view of Lincoln '790

The Examiner admits that Jonsson '888 does not teach translating or updating a memory address. Instead, however, the Examiner asserts that Lincoln '790 teaches to provide an address and compare it with control memory to use the right address for reassembly. Applicants respectfully traverse the rejection on the grounds that there is no basis in fact for combining Jonsson '888 with Lincoln

'790. First, Jonsson '888 does not require address translation, nor would Jonsson '888 ever require memory address translation because Jonsson '888 is silent on the subject of SRAMs and local memories. No address translation is required from the field processors to the combiner, what the Examiner considers to be the next local memory of Jonsson '888. Jonsson '888, more importantly, however, specifically states that "the packet communication path represented by nodes HCN, HDN, and the data path coupled therebetween can be embodied as any type of **point-to-point** packet communication path which utilizes header compression/decompression techniques." (Jonsson '888 at column 3, lines 48-52, emphasis added). Point-to-point packet communication does not require address translation. Jonsson '888 deals only with two header fields, the ID field and the time-to-live/hop-limit (TTL/HL) field, that are problematic during compression and decompression of data packets. Only these fields would be processed in the field processors; there is no suggestion that modification of these fields would require memory translation; in fact, modification of ID fields and TTL/HL fields would not require memory translation. Absent Applicants' teachings and the Examiner's hindsight, there is no motivation to combine Lincoln '790 with Jonsson '888. Please withdraw the rejection of claims 7-8 under 35 U.S.C. §103(a) under Jonsson '888 and Lincoln '790.

The Rejection of claim 11 over Jonsson '888 in view of Li '662

Claim 11 states that the modification to the modifiable portion of the data packet occurs in an ASIC. The Examiner asserts that Jonsson '888 teaches a processing element to perform header modifications but does not specifically teach using an ASIC. Li '662 teaches a hash-caching approach to classify packets for quality of service considerations and teaches that the programmable logic architecture may be rendered as an ASIC. Thus, the Examiner reasons, it would be obvious to have the modification function of Jonsson '888 in an embedded ASIC, and that this modification will render Applicants' claimed invention obvious.

Applicants traverse. There is no motivation to use an ASIC in Jonsson '888 because the circuits that modify the problematic fields of the headers for

compression are relatively simple circuits of comparators, multiplexers, AND gates. *See* Figures 3, 4, 9, 9A, 6, 7, and 7A of Jonsson '888. ASICs are developed for complex circuitry performing complex operations very quickly, such as described in Li '662 that mathematically models internet traffic, creates various weighting factors, the number of consecutive packets in contiguous buckets being up to 800 packets or more, and other quality of service issues, etc. when classifying data packets, *see* column 7, line 57 through column 9, line 63.

Besides, using an ASIC as a field processor in Jonsson '888 still does not create the two additional memories imagined by the Examiner to be obvious to add to Jonsson '888. Li '662 does teach a cache for storing classIDs required for complex quality of service schemes in packet transmission but does not mention forwarding the newly calculated classIDs to the next processor system. Indeed, Li '662 does talk about cache coherency in that if the classID for an incoming packet is not found in the cache, then memory is searched. *See* Li '662, column 2, lines 23-39.Removal of a classID from the cache, moreover, is a complex and integral part of the teaching of Li '662 such that maintaining the cache coherency of Li '662 might require its own processing elements. Thus, neither reference suggests forwarding a modified portion of a packet to a next memory system independent of the unmodified portion of the packet, as Applicants have claimed. Please withdraw the rejection of claim 11 under 35 U.S.C. §103(a) as being obvious in view of Jonsson '888 and Li '662.

The Rejection of claims 13-15, 17-19 over Jonsson '888 in view of Liu '901

The Examiner asserts that Jonsson '888 teaches the apparatus of claim 12 but admits that Jonsson '888 does not teach what type of incoming data would be: analog, digital, optical, etc., the subject of dependent claims 13-15, 17-19. Liu '901 teaches that network interfaces can receive various signals; therefore, the Examiner reasons that it is obvious to receive incoming data that is digital, analog, or optical.

Respectfully, regardless of the type of data that is input into Jonsson '888, Jonsson '888 still does not teach nor suggest: (a) a cache connected to a plurality

of processing elements; (b) a local SRAM memory associated with a destination processing system; and (c) forwarding the unmodified portion of a packet to a destination memory system separate of forwarding the modified portion. Applicants respectfully refer the Examiner to the arguments above with respect to claims 1-6, 9-10, and 12 above. Accordingly, please allow claims 13-15, 17-19.

The Rejection of claim 16 over Jonsson '888 in view of Liu '901 and Lincoln '790

The Examiner rejected claim 16 under 35 U.S.C. §103(a) as being obvious in view of Jonsson '888 in view of Liu '901 and further in view of Lincoln '790. Applicants traverse because Jonsson '888 does not teach modification of the network protocol or a destination address. Jonsson '888 teaches and suggests ONLY modification of problematic fields of a header: an identification field and a TTL/HL field. Lincoln '790 specifically teaches that the modified header and the cell payloads are written to a local memory and that address coherency is maintained between the status queue in host memory and the control queue of a control memory. Nowhere does Jonsson '888, Lincoln '790 or Liu '901 teach modifying a network protocol or changing a destination address and then forwarding the modifications independently of the payload. Recall, that Jonsson '888 and Lincoln '790 forward both the payload and the headers together, regardless of the type of data. Applicants respectfully request the Examiner to withdraw the rejection of claim 16 under 35 U.S.C. §103(a).

Conclusion

Attorney for Applicants thank the Examiner for his review of the amended claims. Applicants amended claims 4 and 6 to overcome the informal objections. With respect to the substantive art rejections, Jonsson '888, being the basis for all the rejections by the Examiner, does not teach or suggest three claimed elements or any need for the changes proposed by the Examiner having the hindsight of Applicants' teachings. Jonsson '888, in particular, does not teach a cache connected to the field processors; Jonsson '888 does not teach or hint at a memory with a destination processing system aka the combiner; and most importantly, Jonsson '888 does not teach or suggest that the modified header is transferred independently of the payload into the combiner. Quite the contrary, the payload and the modified header are transferred together for recombining for compression. Attorney for Applicants requests the Examiner to allow this case which has been pending for four and a half years. Applicants have successfully traversed repeated substantive art rejections based many references; frankly, it is time to allow the amended claims. The Examiner is further invited to telephone the Attorney listed below if he thinks it would expedite the prosecution and the issuance of the patent.

Respectfully submitted,

Date: 01 June 2006 By

Karuna Ojanen
Registration No. 32,484
507.269.6622 voice

IBM Corporation, Dept. 917
3605 Highway 52 North
Rochester, MN 55901-7829